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EXAMINER	
LUU, CUONG V	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,435	BADE ET AL.	
	Examiner	Art Unit	
	Cuong V. Luu	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-78 and 89* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-72,74-78 and 89* is/are rejected.

7)☒ Claim(s) *73* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/19/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 37-78 and 89 are pending. Claims 1-36, 79-88 have been withdrawn. Claim 89 has been added. Claims 37-78 and 89 have been examined. Claim 73 had been objected to. Claims 37-72, 74-78, and 89 have been rejected.

Response to Amendment

1. The amendments on claims 49 and 67 to correct graphical errors have been considered and accepted.

Response to Arguments

2. Applicant's arguments, filed 5/19/2006 page 22, with respect to claim 52 have been considered but are moot in view of the new ground(s) of rejection. Rompaey does teach generating ... a finite state machine (FSM) representation of at least one hardware component, said generating comprising applying a design language having at least one graphical symbol and adapted to form an FSM representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable texture portion defining the behavior of the graphical symbol (p. 8, col. 11, lines 5-6; p. 31, Fig. 11. The recited lines 5-6 on page 8 indicate schematic of a design shown in Fig. 11. The schematic shows symbols of the design with user-definable texture portions defining the behavior of the graphical symbols). Rompaey, however, does not teach creating a virtual test bench using ... of a user interface for each interactive test bench. Cadence Design Systems, Inc., hereafter Cadence, teaches this limitation (Datasheet Interactive Simulation Library, 072597CM5.97, 1997; p. 2, paragraphs 1-3. Since the submitted document has 3 pages but not numbered, the examiner numbers them from 1 to 3 starting from the first

page). It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey and Cadence. Cadence's teachings would have enabled users to examine and appraise a system's performance interactively rather than in "batch-mode" and dramatically accelerated the integration, test and evaluation phase of product development (p. 3, paragraph 1).

3. Applicant's arguments, filed 5/19/2006 page 23, with respect to claims 53-63 have been considered but are moot in view of the new ground(s) of rejection. These claims are argued allowable due to their dependence on claim 52, which is argued allowable. Since claim 52 remains rejected as discussed in item 2, these claims remain rejected.

4. Applicant's arguments, filed 5/19/2006 page 23, with respect to claim 64 have been considered but are moot in view of the new ground(s) of rejection. The arguments of allowance for this claim have already been addressed in item 2 above. This claim, therefore, remains rejected for the same reasons.

5. Applicant's arguments, filed 5/19/2006 page 24, with respect to claims 65-67 have been considered but are moot in view of the new ground(s) of rejection. These claims are argued allowable due to their dependence on claim 64, which is argued allowable. Since claim 64 remains rejected as discussed in item 4, these claims remain rejected.

6. Applicant's arguments, filed 5/19/2006 pages 24-25, with respect to claim 37 have been considered but are moot in view of the new ground(s) of rejection. The arguments of

allowance for this claim have already been addressed in item 2 above. This claim, therefore, remains rejected for the same reasons.

7. Applicant's arguments, filed 5/19/2006 page 25, with respect to claims 38-51 have been considered but are moot in view of the new ground(s) of rejection. These claims are argued allowable due to their dependence on claim 37, which is argued allowable. Since claim 37 remains rejected as discussed in item 6, these claims remain rejected.

8. Applicant's arguments, filed 5/19/2006 pages 26-27, with respect to claim 68 have been considered but are moot in view of the new ground(s) of rejection. The arguments of allowance for this claim have already been addressed in item 2 above. This claim, therefore, remains rejected for the same reasons.

9. Applicant's arguments, filed 5/19/2006 page 27, with respect to claims 69-73 have been considered but are moot in view of the new ground(s) of rejection. These claims are argued allowable due to their dependence on claim 68, which is argued allowable. Since claim 68 remains rejected as discussed in item 8, these claims remain rejected.

10. Applicant's arguments, filed 5/19/2006 pages 27-28, with respect to claim 74 have been considered but are moot in view of the new ground(s) of rejection. The arguments of allowance for this claim have already been addressed in item 2 above. This claim, therefore, remains rejected for the same reasons.

11. Applicant's arguments, filed 5/19/2006 page 28, with respect to claims 75-78 have been considered but are moot in view of the new ground(s) of rejection. These claims are argued allowable due to their dependence on claim 74, which is argued allowable. Since claim 74 remains rejected as discussed in item 10, these claims remain rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 37-39 and 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey (E.U. Application 96870126.8) in view of Cadence (Datasheet Interactive Simulation Library, 072597CM5.97, 1997), and further in view of Hellestrand et al (U.S. Patent 6263302 B1).

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

12. As per claim 37, Rompaey teaches in a computer system having a graphical interface and a design language for forming a finite state machine (FSM) representation of a hardware partition of an embedded system, a method of designing an embedded system, the method comprising:

forming a library of processors including an instruction set accurate simulator for each of the processor cores in the library (col. 9, lines 19-27);

responsive to a first sequence of user commands, selecting at least one of the processor cores from the library as a target processor core (col. 9, lines 23-25);

responsive to a second sequence of user commands, forming a virtual embedded system including an instruction set accurate simulator of a target processor core coupling read, write, and interrupt signals of the instruction set accurate simulator with an FSM simulation of at least one hardware element, wherein generating said FSM ... defining the behavior of the graphical symbol (col. 9, lines 19-22; col. 20, lines 55-58; col. 21, lines 1-14; p. 8, col. 11, lines 5-6; p. 31, Fig. 11. The recited lines 5-6 on page 8 indicate schematic of a design shown in Fig. 11. The schematic shows symbols of the design with user-definable texture portions defining the behavior of the graphical symbols. For example, in Fig. 11, the graphical symbol 104 includes texts 102, 103, and 105 defining its behavior);

responsive to a request from the user, loading an executable binary file of a software application compiled for the target processor core(col. 13, lines 44-52);

executing a simulation of the virtual embedded system running the software application (col. 21, lines 43-47);

Rompaey does not teach:

responsive to a user request, displaying on the GUI a graphical representation of the execution of the software application on the virtual embedded system that includes a software debugger interface to debug the loaded software and a virtual test-bench associated with the GUI and adapted to interact with the simulation, wherein the virtual test-bench is created using a test-bench builder for generating a graphical representation of at least one interactive test-bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for each interactive test bench, to emulate user input to and device output from the virtual embedded system.

Hellestrand et al teach responsive to a user request, displaying on the GUI a graphical representation of the execution of the software application on the virtual embedded system that includes a software debugger interface to debug the loaded software (col. 21, lines 39-59).

Cadence teaches a virtual test-bench associated with the GUI and adapted to interact with the simulation, wherein the virtual test-bench is created using a test-bench builder for generating a graphical representation of at least one interactive test-bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for each interactive test bench, to emulate user input to and device output from the virtual embedded system (p. 2, paragraphs 1-3.)

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, Cadence and Hellestrand et al. Cadence's and Hellestrand et al's teachings would have provided interactive control of the simulation and visual examination of outcome rather than in "batch-mode" and dramatically accelerated the integration, test and evaluation phase of product development (Cadence, p. 3, paragraph 1).

Claims 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey (E.U. Application 96870126.8) in view of Cadence and Hellestrand et al as applied to claim 37 above, and further in view of Schwab (U.S. Pub. 2004/0250083 A1).

13. As per claim 40, Rompaey teaches storing the virtual embedded system as a design (col. 17, lines 49-54),

but not in a design repository coupled to a server; and

providing access privileges to the design to a selected individual or group.

Cadence and Hellestrand et al do not teach this feature either.

Schwab teaches these features (the abstract).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, Cadence, Hellestrand et al, and Schwab. Schwab's teachings would have provided access to a requester, possibly not physically located at the remote terminal, only after verifying that the requester is authorized to view the items (p. 1, paragraph 0002).

14. As per claim 41, Rompaey, Cadence and Hellestrand et al do not teach responsive to a user command, providing access privileges to the design to a group of vendors.

Schwab teaches this feature (the abstract).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, Cadence, Hellestrand et al, and Schwab. Schwab's teachings would have provided access to a requester, possibly not physically located at the remote terminal, only after verifying that the requester is authorized to view the items (p. 1, paragraph 0002).

15. As per claim 42, Rompaey, Cadence and Hellestrand et al do not teach the design is accessible from an on-line bidding board.

Schwab teaches products accessible from an on-line bidding board (p. 10, paragraph 0093).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, Hellestrand et al, Van Huben et al, and Schwab. Schwab's teachings would have made the design available to potential buyers online.

Claims 43-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey (E.U. Application 96870126.8) in view of Cadence and Hellestrand et al as applied to claim 37 above, and Van Huben et al (U.S. Patent 6094654).

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 52-59, 64, and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey in view of Cadence.

16. As per claim 52, Rompaey teaches a computer implemented method of embedded system design, the method comprising:

selecting an instruction set accurate simulator of a target processor core (col. 9, lines 19-27 and 23-25);

generating a virtual hardware component that is a finite state machine (FSM) representation of at least one hardware component ... defining the behavior of the graphical

symbol (col. 9, lines 19-22; col. 20, lines 55-58; col. 21, lines 1-14; p. 8, col. 11, lines 5-6; p. 31, Fig. 11. The recited lines 5-6 on page 8 indicate schematic of a design shown in Fig. 11. The schematic shows symbols of the design with user-definable texture portions defining the behavior of the graphical symbols. For example, in Fig. 11, the graphical symbol 104 includes texts 102, 103, and 105 defining its behavior);

linking read, write, and interrupt signals of the instruction set accurate simulator of the target processor core with corresponding signals of the at least one virtual hardware component to form a virtual embedded system (col. 9, lines 19-22; col. 20, lines 55-58; col. 21, lines 1-14);

coupling a virtual test bench to at least one signal or variable of the virtual embedded system to simulate a human/machine interface (col. 21, lines 8-16); and

coupling a software debugger to the virtual embedded system that is configured to load and run on the virtual embedded system at least one binary program executable of a software application compiled for the target processor core (col. 13, lines 39-48. The applicant mentions Coware, and it inherits software debugger feature).

But does not teach:

Creating a virtual test bench ... to be coupled to a graphical representation of a user interface for each interactive test bench.

Cadence teaches this limitation (p. 2, paragraphs 1-3).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey and Cadence. Cadence's teachings would have provided interactive control of the simulation and visual examination of outcome rather than in "batch-mode" and dramatically accelerated the integration, test and evaluation phase of product development (Cadence, p. 3, paragraph 1).

17. As per claim 53, Rompaey teaches selecting the target processor core from a library having a plurality of instruction set accurate simulators for a plurality of processor cores (col. 9, lines 19-27).

18. As per claim 54, Rompaey teaches selecting the virtual hardware component from a library of virtual hardware components (col. 9, lines 23-25).

19. As per claim 55, Rompaey teaches modifying the virtual hardware component (col. 7, lines 43-55).

20. As per claim 56, Rompaey teaches loading benchmark software in an evaluation phase of an embedded system project and running a simulation of the virtual embedded system executing the benchmark software (col. 10, lines 10-13. Benchmark software is a type of application software. Therefore, the examiner interprets Rompaey suggests a benchmark software to be executed on the virtual embedded system).

21. As per claim 57, Rompaey teaches loading binary program executables of development software compiled for the target processor core in a development phase of an embedded systems project and running a simulation of the virtual embedded system executing the development software (col. 10, lines 10-13).

22. As per claim 58, this limitation has already been discussed in claim 52. It is, therefore, rejected for the same reasons.

23. As per claim 59, Rompaey teaches storing the virtual embedded system as a design having at least one executable file in a design repository (col. 17, lines 49-54l col. 32, lines 41-47).

24. As per claim 64, Rompaey teaches a method of designing an embedded system, the method comprising:

defining a system architecture of the embedded system (col. 7, lines 31-35);

generating a finite state machine (FSM) representation of at least one hardware element ... defining the behavior of the graphical symbol (col. 9, lines 19-22; col. 20, lines 55-58; col. 21, lines 1-14; p. 8, col. 11, lines 5-6; p. 31, Fig. 11. The recited lines 5-6 on page 8 indicate schematic of a design shown in Fig. 11. The schematic shows symbols of the design with user-definable texture portions defining the behavior of the graphical symbols);

designing a virtual prototype of the embedded system having an instruction set accurate simulator of a target processor core coupling read, write, and interrupt signals of the instruction set accurate simulator with said FSM representation of at least one hardware element (col. 20, lines 55-58; col. 21, lines 1-14);

coupling the virtual prototype to a software debugger having a debugging interface and to the virtual test bench (col. 9, lines 19-22; col. 13, lines 39-48. The applicant mentions Coware, and it inherits graphical interface with the embedded system);

developing at least one software application for the processor core (col. 10, lines 10-13);

loading compiled binary program code compiled from the at least one software application for execution of the virtual prototype (col. 10, lines 10-13); and

initiating a simulation of the virtual prototype executing the at least one software application (col. 10, lines 10-13).

But does not teach:

Creating a virtual test bench ... to be coupled to a graphical representation of a user interface for each interactive test bench.

Cadence teaches this limitation (p. 2, paragraphs 1-3).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey and Cadence. Cadence's teachings would have provided interactive control of the simulation and visual examination of outcome rather than in "batch-mode" and dramatically accelerated the integration, test and evaluation phase of product development (Cadence, p. 3, paragraph 1).

25. As per claim 89, Cadence teaches the step of interacting at run time with the virtual prototype to simulate an application of the embedded system (p. 2, paragraph 3. In this paragraph Cadence teaches the interactive control when running the simulation. This is regarded as interacting at run time with the virtual prototype to simulate an application of the embedded system).

Claims 60-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey in view of Cadence as applied to claims 52 and 59 above, and further in view of Van Huben et al.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim 65-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey in view of Cadence as applied to claim 64 above, and further in view of Schubert et al (U.S. Pub. 2005/0193280 A1).

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 68-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey in view of Cadence and further in view of Van Huben et al.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

26. As per claim 68, Rompaey teaches a method of providing information to potential suppliers for procuring a good or service associated with an embedded system, the method comprising:

defining a system architecture of the embedded system (col. 7, lines 31-35);

designing a virtual prototype of the embedded system, the virtual prototype having an instruction set accurate simulator of a target processor core, wherein generating said FSM ... a user-definable texture portion defining the behavior of the graphical symbol (col. 20, lines 55-58; col. 21, lines 1-14; p. 8, col. 11, lines 5-6; p. 31, Fig. 11);

coupling the virtual prototype to a virtual test bench having a graphical representation of a human/machine interface for interacting with the embedded system (col. 9, lines 19-22;

col. 13, lines 39-48. The applicant mentions Coware, and it inherits graphical interface with the embedded system);

Rompaey does not teach:

creating a virtual test bench ... a user interface for each interactive test bench; and

publishing the virtual prototype as a functional specification from which a vendor may initiate a simulation of the operation of the embedded system.

Cadence teaches creating a virtual test bench ... a user interface for each interactive test bench (p. 2, paragraphs 1-3);

Van Huben et al teach making a design available to a selected individual or group to dispatch tasks on it (col. 29, lines 54-59; col. 15, lines 48-55).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Rompaey, Cadence and Van Huben et al. Cadence's and Van Huben et al's teachings would have provided interactive control of the simulation and visual examination of outcome rather than in "batch-mode" and dramatically accelerated the integration, test and evaluation phase of product development and access of the stored embedded system for reuse to a selected group or people.

Claims 71-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rompaey in view of Cadence and Van Huben et al as applied to claims 68 and 70 above, and further in view of Schwab.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 74 and 76-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Huben et al in view of Rompaey and further in view of Cadence.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

27. As per claim 74, Van Huben et al teach a computer-implemented method for a vendor to acquire information for the procurement of a service related to a project, the method comprising:

accessing a database of a design (col. 29, lines 55-59);

instantiating an instance of one of the virtual prototypes (col. 15, lines 48-53); and

evaluating the virtual prototype (col. 15, lines 48-53).

But Van Huben et al do not teach:

The design being a virtual prototype of embedded system, each of the virtual prototypes having a processor simulator, a finite state machine representation of hardware peripherals, and a virtual test bench emulating a human/machine interface for interacting with a simulation of the operation of the virtual prototype.

Wherein generating said FSM representation ... defining the behavior of the graphical symbol, and

Wherein the virtual test bench ... a user interface for the interactive test bench;

Rompaey teaches the design being a virtual prototype of embedded system, each of the virtual prototypes having a processor simulator, a finite state machine representation of hardware peripherals, and a virtual test bench emulating a human/machine interface for

interacting with a simulation of the operation of the virtual prototype (col. 20, lines 55-58; col. 21, lines 1-14; col. 9, lines 19-22; col. 13, lines 39-48).

Wherein generating said FSM representation ... defining the behavior of the graphical symbol (p. 8, col. 11, lines 5-6; p. 31, Fig. 11).

Cadence teaches wherein the virtual test bench ... a user interface for the interactive test bench (p. 2, paragraphs 1-3).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Van Huben et al, Rompaey and Cadence. Rompaey's and Cadence's teachings would have made a virtual prototype of embedded system accessible for evaluation and provided interactive control of the simulation and visual examination of outcome rather than in "batch-mode" and dramatically accelerated the integration, test and evaluation phase of product development.

Claims 75 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Huben et al in view of Rompaey and Cadence as applied to claim 74 above, and further in view of Schwab.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Allowable Subject Matter

Claim 73 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

28. Claim 73 is indicated allowable because the prior arts do not teach the virtual prototype is published to a database having a matching engine.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong V. Luu whose telephone number is 571-272-8572. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah, can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. An inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CVL

KAMINI SHAH
SUPERVISORY PATENT EXAMINER